VLSI M.Tech/M.E IEEE Projects List

2018 IEEE TRANSACTIONS		
S.No	**Title**	**Tool**
1	Efficient Protection of the Register File in Soft-processors Implemented on Xilinx FPGAs	XILINX
2	FIR Filter Realization via Deferred End-Around Carry Modular Addition	XILINX
3	Low-Complexity VLSI Design of Large Integer Multipliers for Fully Holomorphic Encryption	XILINX
4	Advanced Compressor Tree Synthesis for FPGAs	XILINX
5	Approximate DCT Image Compression using Inexact Computing	XILINX
6	Compact CA-Based Single Byte Error Correcting Codec	XILINX
7	DuCNoC: A High-Throughput FPGA-based NoC simulator using Dual-Clock Lightweight Router Micro-Architecture	XILINX
8	A Single and Adjacent Error Correction Code for Fast Decoding of Critical Bits	XILINX
9	FIR Filter Realization via Deferred End-Around Carry Modular Addition	XILINX
10	VLSI Design and Implementation of Reconfigurable 46-Mode Combined-Radix-Based FFT Hardware Architecture for 3GPP-LTE Applications	XILINX
11	Vector Processing-Aware Advanced Clock-Gating Techniques for Low-Power Fused Multiply-Add	XILINX
12	Bit stream Fault Injections (BiFI)– Automated Fault Attacks against SRAM-based FPGAs	XILINX
13	An Efficient Fault-Tolerance Design for Integer Parallel Matrix–Vector Multiplications	XILINX

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14	Approximate Hybrid High Radix Encoding for Energy-Efficient Inexact Multipliers	XILINX
15	Detection and diagnosis of single faults in quantum circuits	XILINX
16	Randomized Mixed-Radix Scalar Multiplication	XILINX
17	VLSI Design of SVM-Based Seizure Detection System With On-Chip Learning Capability	XILINX
18	YodaNN1: An Architecture for Ultra-Low Power Binary-Weight CNN Acceleration	XILINX
19	A Scheme to Design Concurrent Error Detection Techniques for the Fast Fourier Transform Implemented in SRAM-based FPGAs	XILINX
20	Optimizing the Convolution Operation to Accelerate Deep Neural Networks on FPGA	XILINX
21	GliFreD: Glitch-Free Duplication Towards Power-Equalized Circuits on FPGAs	XILINX
22	Solving Large Problem Sizes of Index-Digit Algorithms on GPU: FFT and Tridiagonal System Solvers	XILINX
23	Unbiased Rounding for HUB Floating-point Addition	XILINX
24	Accelerating FV Homomorphic scheme in FPGA with Karatsuba algorithm	XILINX
25	FFT-based McLaughlin's Montgomery Exponentiation without Conditional Selections	XILINX
26	A Multiplexer-Based Arbiter PUF Composition with Enhanced Reliability and Security	XILINX
27	STABLE: **St**ress-**a**ware **B**oo**le**an Matching to Mitigate BTI-induced SNM Reduction in SRAM-based FPGAs	XILINX

28	Approximate Sum-of-Products Designs Based on Distributed Arithmetic	XILINX
29	High-Performance Architecture Using Fast Dynamic Reconfigurable Accelerators	XILINX
30	Low-Power and Fast Full Adder by Exploring New XOR and XNOR Gates	XILINX
31	Systematic Design of an Approximate Adder: The Optimized Lower Part Constant-OR Adder	XILINX
32	A Simple Yet Efficient Accuracy-Configurable Adder Design	XILINX
33	Optimal Single Constant Multiplication Using Ternary Adders	XILINX
34	RAP-CLA: A Reconfigurable Approximate Carry Look-Ahead Adder	XILINX
35	Decimal Full Adders Specially Designed for Quantum-Dot Cellular Automata	XILINX
36	A Low-Error Energy-Efficient Fixed-Width Booth Multiplier With Sign-Digit-Based Conditional Probability Estimation	XILINX
37	Design of Area-Efficient and Highly Reliable RHBD I0T Memory Cell for Aerospace Applications	TANNER/ MICROWIND
38	A Time-Efficient CMOS-Memristive Programmable Circuit Realizing Logic Functions in Generalized AND–XOR Structures	TANNER/ MICROWIND
39	Multilevel Half-Rate Phase Detector for Clock and Data Recovery Circuits	TANNER/ MICROWIND
40	Input Offset Estimation of CMOS Integrated Circuits in Weak Inversion	TANNER/ MICROWIND
2018 IEEE JOURNALS/CONFERENCES		
41	An Approach to LUT Based Multiplier for Short Word Length DSP Systems	XILINX

42	FPGA Implementation of an Improved Watchdog Timer for Safety-critical Applications	XILINX
43	EEG Signal Denoising based on Wavelet Transform using Xilinx System Generator.	XILINX
44	Tap Delay-and-Accumulate Cost Aware Coefficient Synthesis Algorithm for the Design of Area-Power Efficient FIR Filters.	XILINX
45	Area and Power Efficient VLSI Architecture of Distributed Arithmetic Based LMS Adaptive Filter	XILINX
46	VLSI Design Of Low-Cost And High-Precision Fixed-Point Reconfigurable FFT Processors	XILINX
47	A Low-Power High-Speed Accuracy-Controllable Approximate Multiplier Design	XILINX
48	Chip Design for Turbo Encoder Module for In-Vehicle System	XILINX
49	Low-power Implementation of Mitchell's Approximate Logarithmic Multiplication for Convolutional Neural Networks	XILINX
50	Novel High speed Vedic Multiplier proposal incorporating Adder based on Quaternary Signed Digit number system	XILINX
51	The Design and Implementation of Multi – Precision Floating Point Arithmetic Unit Based on FPGA	XILINX
52	An Efficient VLSI Architecture for Convolution Based DWT Using MAC	XILINX
53	Extending 3-bit Burst Error-Correction Codes With Quadruple Adjacent Error Correction	XILINX
54	A Low-Power Yet High-Speed Configurable Adder for Approximate Computing	XILINX
55	Efficient Modular Adders based on Reversible Circuits	XILINX
56	Binary To Gray Code Converter Implementation Using QCA	XILINX
57	Power Efficient Approximate Multipliers in LMS Adaptive Filters	XILINX
58	MAES: Modified Advanced Encryption Standard for Resource Constraint Environments	XILINX
59	A Novel Design of Flip-Flop Circuits using Quantum Dot Cellular Automata (QCA)	XILINX

60	High Performance Division Circuit using Reversible Logic Gates	XILINX
61	A Novel Five-input Multiple-function QCA Threshold Gate	TANNER/ MICROWIND
62	A Low-Power High-Speed Comparator for Precise Applications	TANNER/ MICROWIND
63	A High Performance Gated Voltage Level Translator with Integrated Multiplexer	TANNER/ MICROWIND
64	High speed and low power preset-able modified TSPC D flip-flop design and performance comparison with TSPC D flip-flop	TANNER/ MICROWIND
65	Low Leakage Fully Half-Select-Free Robust SRAM Cells with BTI Reliability Analysis	TANNER/ MICROWIND
	2017 IEEE TRANSACTIONS	
66	A Bit-Plane Decomposition Matrix-Based VLSI Integer Transform Architecture for HEVC	XILINX
67	Probability-Driven Multibit Flip-Flop Integration With Clock Gating	XILINX
68	Area-Time Efficient Architecture of FFT-Based Montgomery Multiplication	XILINX
69	Reliable Low-Latency Viterbi Algorithm Architectures Benchmarked on ASIC and FPGA	XILINX
70	Improved 64-bit Radix-16 Booth Multiplier Based on Partial Product Array Height Reduction	XILINX
71	A Structured Visual Approach to GALS Modeling and Verification of Communication Circuits	XILINX
72	Weighted Partitioning for Fast Multiplierless Multiple-Constant Convolution Circuit	XILINX
73	Low-Latency, Low-Area, and Scalable Systolic-Like Modular Multipliers for GF(2^m) Based on Irreducible All-One Polynomials	XILINX
74	Probabilistic Error Modeling for Approximate Adders	XILINX

75	LFSR-Based Generation of Multicycle Tests	XILINX
76	Clock-Gating of Streaming Applications for Energy Efficient Implementations on FPGAs	XILINX
77	An Improved DCM-Based Tunable True Random Number Generator for Xilinx FPGA	XILINX
78	RoBA Multiplier: A Rounding-Based Approximate Multiplier for High-Speed yet Energy-Efficient Digital Signal Processing	XILINX
79	DLAU: A Scalable Deep Learning Accelerator Unit on FPGA	XILINX
80	A 4096-Point Radix-4 Memory-Based FFT Using DSP Slices	XILINX
81	Design of Efficient Multiplierless Modified Cosine-Based Comb Decimation Filters: Analysis and Implementation	XILINX
82	Efficient Hardware Implementation of Probabilistic Gradient Descent Bit-Flipping	XILINX
83	Design of Efficient BCD Adders in Quantum-Dot Cellular Automata	XILINX
84	Overloaded CDMA Crossbar for Network-On-Chip	XILINX
85	High-Throughput and Energy-Efficient Belief Propagation Polar Code Decoder	XILINX
86	Design of Power and Area Efficient Approximate Multipliers	XILINX
87	An Efficient O(N) Comparison-Free Sorting Algorithm	XILINX
88	Energy-Efficient VLSI Realization of Binary64 Division With Redundant Number Systems	XILINX
89	A General Digit-Serial Architecture for Montgomery Modular Multiplication	XILINX
90	High-Speed Parallel LFSR Architectures Based on Improved State-Space Transformations	XILINX
91	Scalable Approach for Power Droop Reduction During Scan-Based Logic BIST	XILINX
92	Sign-Magnitude Encoding for Efficient VLSI Realization of Decimal Multiplication	XILINX
93	A Memory-Based FFT Processor Design With Generalized Efficient Conflict-Free Address Schemes.	XILINX
94	On the VLSI Energy Complexity of LDPC Decoder Circuits	XILINX

95	Reconfigurable Constant Multiplication for FPGAs	XILINX
96	LLR-Based Successive-Cancellation List Decoder for Polar Codes With Multibit Decision	XILINX
97	Area-Efficient Architecture for Dual-Mode Double Precision Floating Point Division	XILINX
98	Digit-Level Serial-In Parallel-Out Multiplier Using Redundant Representation for a Class of Finite Fields.	XILINX
99	Dual-Quality 4: 2 Compressors for Utilizing in Dynamic Accuracy Configurable Multipliers	TANNER/ MICROWIND
100	Low-Power Design for a Digit-Serial Polynomial Basis Finite Field Multiplier Using Factoring Technique	TANNER/ MICROWIND
101	Design of Low-Power High-Performance 2-4 and 4-16 Mixed-Logic Line Decoders.	TANNER/MW
102	Register-Less NULL Convention Logic.	TANNER/ MICROWIND
103	Design of Defect and Fault-Tolerant Nonvolatile Spintronic Flip-Flops	TANNER/ MICROWIND
104	Delay Analysis for Current Mode Threshold Logic Gate Designs	TANNER/ MICROWIND
105	10T SRAM Using Half-V_{DD} Precharge and Row-Wise Dynamically Powered Read Port for Low Switching Power and Ultralow RBL Leakage	TANNER/ MICROWIND